

Xiaoyu Zheng

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EDUCATION

Harbin Institute of Technology 08/2021-06/2025

- B.Eng. Microelectronics Science & Engineering

University of Southampton 09/2025-09/2026

- MSc. Microelectronics Systems Design

PUBLICATIONS

- X. Zheng, Z. Guo, C. Zhou#, "A Unified Function Processor with Integer Arithmetic Based on Piecewise Chebyshev Polynomial Approximation", *IEEE ISCAS*, 2026.
- C. Zhou#, X. Zheng, Z. Guo, "Variable Bit-Width Unified Function Processor for AI Acceleration", *IEEE Transactions on Circuits and Systems I (TCAS-I)*, in preparation.
- X. Zheng, K. Zhou, C. Zhou#, "Voxel-Based Point Cloud Processing Architecture for Hardware Acceleration", *IEEE Transactions on Circuits and Systems II (TCAS-II)*, in preparation.

RESEARCH EXPERIENCES

A Unified Function Processor with Integer Arithmetic Based on Piecewise Chebyshev Polynomial Approximation (Under the supervision of Dr. Changchun Zhou) 07/2025 –Present

- Proposed the Quantization-Aware Polynomial Approximation Algorithm (QADP) based on Chebyshev, integrating segmentation and quantization via a two-layer dynamic programming framework.
- Built a configurable Python toolchain for design-space exploration and error-resource trade-off analysis.

Voxel-based Point Cloud Processing for Hardware Acceleration 09/2024-Present

- Designed a point cloud sampling and neighbor-search algorithm based on voxel partitioning, replacing traditional FPS/KNN distance calculations with voxel index lookups;
- Reduced explicit distance computations by leveraging voxel index mapping;

PROJECT EXPERIENCES

Volans LLM Chip (Under the supervision of Dr. Changchun Zhou)

Team Member (NPU Subsystem Microarchitecture Co-designer and Developer) 2/2026-Present

- Co-designed the microarchitecture of a research-oriented LLM accelerator;
- Co-designed an 8-stage AXI-Stream-based streaming datapath with stage-level functional partitioning;
- Designing and implementing compute modules at RTL level.

Fornax Diffusion Chip (Under the supervision of Dr. Changchun Zhou)

Team Member (OCI Module Developer, UFP Module Co-developer) 12/2025-Present

- Designed the OCI (output reversely compresses input) module, including module-level instruction registers configuration, micro-architecture design, dataflow, and RTL implementation;
- Designed a pipeline covering AXI transactions, address generation, data reorganization and scheduling;
- Completed module-level simulation and functional verification, finally integrated the module with CCU/AXI subsystems within the SoC.

Research on Intelligent Control and Application of Landscape Lighting in Complex Environments

Team Member of Controller Part (Provincial-level Project) 10/2024-06/2025

- Developed a dynamic audio-responsive lighting control system based on feature extraction and adaptive control algorithms;
- Implemented Modbus protocol, ADC acquisition, and RS485 communication on STM32 platform;
- Deployed in the 2025 Harbin Ice and Snow World

SKILLS

- **Programming:** Verilog, SystemVerilog, C, Python
- **Digital ASIC Implementation:** Basic Full RTL-to-GDSII flow; Synopsys DC/DFT, Cadence Xcelium/Innovus/ Virtuoso; AMS 0.35 μ m/TSMC 180nm PDK; SDC constraints; post-layout simulation
- **FPGA & Embedded & Simulation:** Quartus, ModelSim, MATLAB, Altium Designer